

Amendments to the Claims:

This listing of claims replaces all prior versions, and listings, of claims in this application.

Listing of Claims:

1. (Currently Amended) A microelectronic structure, comprising:
 - a substrate comprising circuits;
 - a plurality of ~~conductive bumps provided in adjacent relationship to each other~~ on the substrate ~~in electrical contact with the circuits~~, each of the plurality of ~~conductive bumps including an~~ being electrically insulative layer and having an upper surface, a pair of sidewalls, an outer wall facing away a center portion of the substrate and an inner wall facing towards the center portion of the substrate and connected to the outer wall by the pair of sidewalls; and
 - a conductive layer provided over ~~the electrically insulative layer of each of the plurality of conductive bumps~~ extending from the upper surface to the circuits,
 - wherein the conductive layer is absent from at least one of the pair of sidewalls of each of the plurality of bumps.
2. (Previously Presented) The microelectronic structure of claim 1, wherein the conductive layer is absent from both of the pair of sidewalls.
3. (Previously Presented) The microelectronic structure of claim 1, further comprising at least one shoulder provided in the conductive layer at the upper surface.
4. (Cancelled)
5. (Previously Presented) The microelectronic structure of claim 1, wherein the conductive layer is absent from the inner wall.
6. (Previously Presented) The microelectronic structure of claim 5, wherein the conductive layer is absent from both of the pair of sidewalls.
7. (Previously Presented) The microelectronic structure of claim 5, further comprising at least one shoulder provided in the conductive layer at the upper surface.

8. (Cancelled)

9. (Previously Presented) The microelectronic structure of claim 1, wherein the conductive layer is formed of a conductive metal selected from the group consisting of Au, Ag, Pt, Pd, Al, Cu, Sn and alloys thereof.

10. (Previously Presented) The microelectronic structure of claim 9, wherein the conductive layer is absent from both of the pair of sidewalls.

11. (Previously Presented) The microelectronic structure of claim 9, further comprising at least one shoulder provided in the conductive layer at the upper surface.

12. (Cancelled)

13. (Currently Amended) A microelectronic structure, comprising:

a substrate comprising circuits;

a plurality of ~~conductive bumps provided in adjacent relationship to each other~~ in rows on the substrate ~~and in electrical contact with said circuits~~, each of the plurality of ~~conductive bumps including an~~ being electrically insulative layer and having an upper surface, a pair of sidewalls, an outer wall facing away a center portion of the substrate and an inner wall facing towards the center portion of the substrate and connected to the outer wall by the pair of sidewalls;

a conductive layer provided over ~~the electrically insulative layer of each of the plurality of conductive bumps~~ extending from the upper surface to the circuits, wherein the conductive layer is absent from at least one of the pair of sidewalls of each of the plurality of bumps; and

a protection layer provided on the substrate ~~adjacent to~~ near the rows of the plurality of ~~conductive bumps~~.

14. (Previously Presented) The microelectronic structure of claim 13, wherein the conductive layer is absent from both of the pair of sidewalls.

15. (Previously Presented) The microelectronic structure of claim 13, wherein the conductive layer is absent from the inner wall.

16. (Currently Amended) The microelectronic structure of claim 13, further comprising a ~~test~~ probe pad provided on the substrate adjacent to near each one of the plurality of ~~conductive~~ bumps and in electrical contact with the conductive layer.

17. (Withdrawn) A method of fabricating a conductive bump on a substrate, comprising the steps of:

providing a substrate comprising circuits;

providing a bump-forming structure having an upper surface, a pair of sidewalls, an outer wall and an inner wall on said substrate in electrical contact with said circuits;

providing a conductive layer on said bump-forming structure; and

removing said conductive layer from at least one of said sidewalls.

18. (Withdrawn) The method of claim 17 further comprising the step of removing said conductive layer from both of said sidewalls.

19. (Withdrawn) The method of claim 17 further comprising the step of removing said conductive layer from said outer wall.

20. (Withdrawn) The method of claim 17 further comprising the step of providing at least one shoulder in said conductive layer at said upper surface.

21. (Currently Amended) A microelectronic structure, comprising:

a substrate comprising circuits;

a plurality of ~~conductive~~ bumps formed on the substrate, each of the plurality of ~~conductive~~ bumps including an being electrically insulative layer and having an upper surface and a side surface; and

a conductive layer formed over ~~the electrically insulative layer of~~ each of the plurality of ~~conductive~~ bumps extending from the upper surface to the circuits, exposing at least one portion of the side surface of each of the plurality of bumps.

22. (Previously Presented) The microelectronic structure of claim 21, wherein the conductive layer exposes at least one portion of the upper surface.

23. (Currently Amended) The microelectronic structure of claim 21, wherein the plurality of ~~conductive~~ bumps are formed in rows in a staggered pattern ~~one row to another~~.

24. (Currently Amended) The microelectronic structure of claim 21, wherein the conductive layer exposes ~~the~~ a portion of the side surface of ~~the electrically insulative layer of~~ at least one of the plurality of ~~conductive~~ bumps that faces towards a center portion of the substrate.

25. (Currently Amended) The microelectronic structure of claim 21, wherein the conductive layer exposes at least one of the side surfaces of ~~the electrically insulative layers of~~ two immediately adjacent ~~conductive~~ bumps of the plurality of bumps.

26. (Previously Presented) The microelectronic structure of claim 21, wherein the conductive layer extends from the upper surface via a portion of the side surface to the substrate and extends further over the substrate.

27. (Currently Amended) A semiconductor package, comprising:

- a first substrate;

- a plurality of conductive pads formed on the first substrate;

- a microelectronic structure including:

- a second substrate comprising circuits;

- a plurality of ~~conductive~~ bumps formed on the substrate corresponding to the plurality of conductive pads, each of the plurality of ~~conductive~~ bumps ~~including an~~ being electrically insulative ~~layer~~ and having an upper surface and a side surface; and

a conductive layer formed over ~~the electrically insulative layer of~~ each of the plurality of ~~conductive~~ bumps extending from the upper surface to the circuits, exposing at least one portion of the side surface of each of the plurality of bumps; and

a film disposed between the first substrate and the second substrate ~~for electrically to facilitate~~ connecting the plurality of ~~conductive~~ bumps to the plurality of conductive pads.

28. (Previously Presented) The semiconductor package of claim 27, wherein the conductive layer exposes at least one portion of the upper surface.

29. (Currently Amended) The semiconductor package of claim 27, wherein the plurality of ~~conductive~~ bumps are formed in rows in a staggered pattern ~~one row to another~~.

30. (Currently Amended) The semiconductor package of claim 27, wherein the conductive layer exposes ~~the~~ a portion of the side surface of ~~the electrically insulative layer of~~ at least one of the plurality of ~~conductive~~ bumps that faces towards a center portion of the substrate.

31. (Currently Amended) The semiconductor package of claim 27, wherein the conductive layer exposes at least one of the side surfaces of ~~the electrically insulative layers of~~ two immediately adjacent ~~conductive~~ bumps of the plurality of bumps.

32. (Previously Presented) The semiconductor package of claim 27, wherein the conductive layer extends from the upper surface via a portion of the side surface to the substrate and extends further over the substrate.

33. (Currently Amended) The semiconductor package of claim 27, wherein the film includes one of an anisotropic conducting film ~~or~~ and a non-conductive film.

34. (Currently Amended) The semiconductor package of claim 27, wherein each of the ~~electrically insulative layer~~ plurality of bumps includes polyimide.